【Grant-in-Aid for Scientific Research (S)】

Creation and development of superconducting computing technology for post-Moore era

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Purpose and Background of the Research

●Outline of the Research

Although device research was active worldwide toward realizing a superconductor computer about 30 years ago, it entered a winter era, unfortunately. However, this phase is now undergoing a significant change. This is because, in addition to advances in materials and circuits of superconductor technologies, research in superconductor computer architecture has advanced dramatically in recent years. Under these circumstances, superconductor computing is again attracting attention as one of the most promising candidates for the next-generation computing infrastructure. We have led the world in Single Flux Quantum (SFQ) circuits and architecture. We have successfully demonstrated a 32-GHz bit-parallel SFQ processor and a 34-GHz AI accelerator prototype for the first time in the world. This research aims to enhance such cutting-edge SFQ technologies to a system level and establish them as the world's first general-purpose computing technology with cryogenic superconductivity (Figure 1).

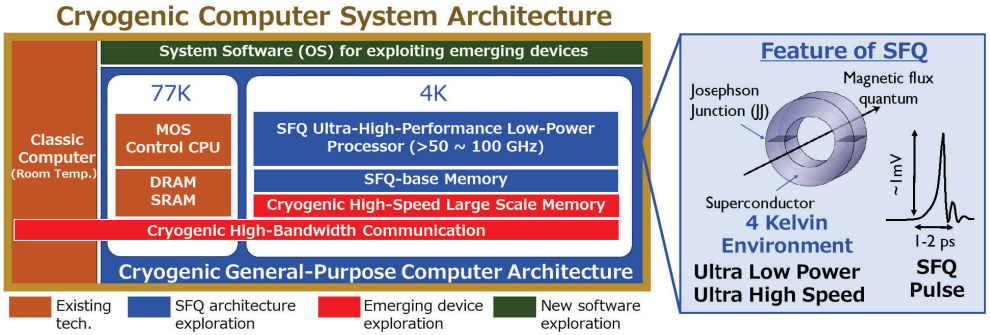

Figure 1. Overview of this research (SFQ logic and cryogenic computer system architecture)

●Research Theme (1/3): Cryogenic Superconductor Device Technology

Based on the cutting-edge SFQ technologies, we introduce new principles and develop novel emerging devices for advanced SFQ computing as follows.

- ❖ Memory: To solve a memory problem fundamentally, we explore a new magnetic memory cell structure that achieves high capacity (high integration) while maintaining the ultra-high speed that is a feature of SFQ processors.
- ❖ Communication: To transmit information of the ultra-weak pulse signal, which is the information carrier of the SFQ circuit, we explore a new optical transistor device that realizes to convert the SFQ pulses to optical information efficiently.
- ❖ Computation: To overcome the current limitation in conservative designs, we explore a new SFQ circuit that aggressively reduces the design margins and constraints for maximizing power-performance efficiency.

●Research Theme (2/3): Cryogenic Superconductor Computer Architecture Technology

We devise an innovative SFQ computer architecture significantly different from conventional ones. Based on the new concept of "maximizing the advantages of novel devices while concealing their disadvantages," we explore the following architectural techniques through cross-disciplinary collaboration between devices and architectures (Figure 2).

- ❖ Theoretical construction of spatial-temporal information representation method: We attempt to combine spatial and temporal information representation for SFQ logic, construct its mathematical theory and explore the arithmetic/memory circuits.
- ❖ Cryogenic SFQ processor architecture: We propose a novel architecture consisting of a cryogenic low-speed exact processing part using MOS-FETs and a cryogenic ultra-high-speed exact/non-exact processing part using SFQs.
- ❖ Cryogenic memory architecture: A new hierarchical memory structure is derived using new cryogenic memory devices.

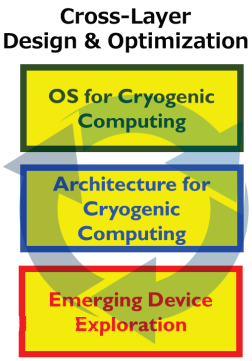

Figure 2. Device and Architecture Co-design

●Research Theme (3/3): Cryogenic System Software (OS) Technology

Explore operating system technologies that effectively use and manage cryogenic hardware resources.

- ❖ Run-time bias-voltage/operating-frequency control technology: Explore DbVFS (Dynamic bias-Voltage and Frequency Scaling) technology for SFQs that optimizes supply voltage and operating frequency.
- ❖ Runtime Cooling Temperature Management Techniques: Explore thermal control techniques for SFQ logics that optimize the trade-off between error frequency and cooling cost.

Expected Research Achievements

●Emerging Devices

We contribute to creating cryogenic devices by verifying the operating principles and establishing the scientific theories of novel cryogenic devices for next-generation SFQ computing.

●SFQ Computer Architecture

We devise novel architectures for classical superconductor computing (Figure 1). The feasibility and effectiveness are demonstrated through prototype chip designs and system-level simulations. We also establish a computer design method with emerging devices (Figure 3).

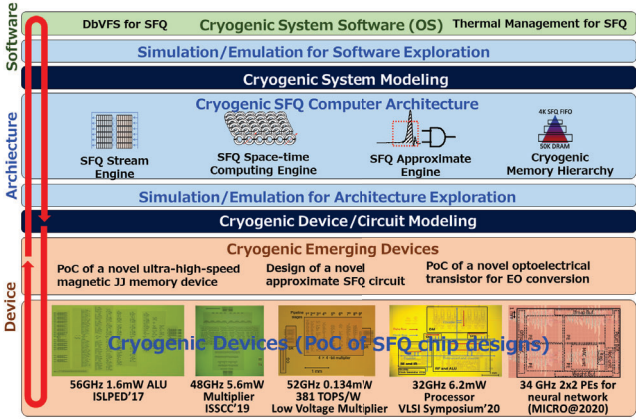

Figure 3. Computer Design Methodology in Post-Moore Era

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