【Grant-in-Aid for Scientific Research(S)】
Science and Engineering (Engineering Ⅱ)

# Title of Project : Principles for the development of a diffusion barrier layer to overcome the process limitations of multi-layer interconnects for semiconductor devices

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Research Area : Engineering

Keyword : Interconnect, copper alloy, semiconductor, barrier layer, field-enhanced growth

## 【Purpose and Background of the Research】

Advanced LSI devices require thin-film diffusion barrier layers at various hetero-interfaces. Since the thickness of the barrier layer should be less than several nm, the control of barrier thickness and properties is extremely difficult. In addition, fundamental principles of the barrier formation are not understood. Based on our previous research, the growth of the barrier layer is related to field-enhanced diffusion induced by electron tunneling. This work further investigate the relation between the electron tunneling and the electron energy band structure across the barrier layer. The obtained results will serve to establish fundamental principles for the formation of diffusion barrier layers in various devices.

## 【Research Methods】

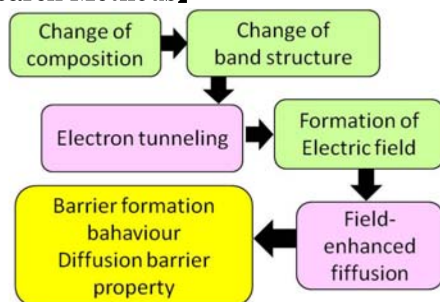


Fig. 1 Schematic of research methods

Various Cu alloys will be thermally reacted with $SiO_2$ and the following items will be investigated.

(1) Chemical composition of the interface layer and $SiO_2$
(2) Energy band structure and the presence of the occupation sites of tunneling electrons
(3) Ionization state of the constituent elements and the formation of electric field across the interface layer
(4) Growth behavior and diffusion barrier property of the interface layer.

The necessary conditions to self-form a diffusion barrier and its formation mechanism will be understood by considering interrelation among composition change, band structure change, electron tunneling, field formation, and field-enhanced diffusion.

## 【Expected Research Achievements and Scientific Significance】

This research will provide fundamental principles to control chemical, mechanical, and electrical properties of hetero-interfaces. Based Based on the obtained results, we can overcome overcome technical challenges associated with the fabrication of advanced LSI devices. It It is also possible to provide vital information information for the development of various various devices, such as oxide TFT, MIM capacitors, MRAM, and any hetero structures which require nano-scale interface.

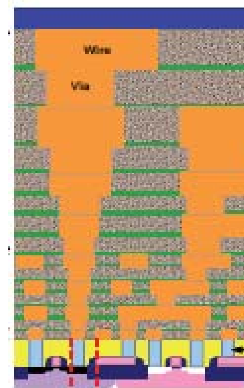


Fig. 2 Interconnect structure (from ITRS roadmap)

## 【Publications Relevant to the Project】

・"Graded composition and valence states in self-forming barrier layers at Cu-Mn/SiO2 interface", Y. Otsuka et al., Appl. Phys. Lett., 96, 012101 (2010).
・"Growth kinetics and thermal stability of a self-formed barrier layer at Cu-Mn/SiO2 interface", J. Koike et al., J. Appl. Phys. 102, 043527 (2007).

## 【Term of Project】 FY2010-2014

## 【Budget Allocation】 81,700 Thousand Yen

## 【Homepage Address and Other Contact Information】

http://www.material.tohoku.ac.jp/~kyokugen/lab.html