【Grant-in-Aid for Scientific Research(S)】

Science and Engineering (Engineering I)

Title of Project : Three-Dimensionally Stacked Optoelectronic System-on-Chip Fabricated Using Grapho-Assembly

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Research Area : Engineering

Keyword : Electronic Devices and Integrated Circuit

【Purpose and Background of the Research】

The performance and integration capacity of LSIs have been significantly improved by scaling-down the transistor size. However, several issues such as the increased power consumption and the statistical variations of device properties have become more serious as the device size is reduced. Meanwhile the demand for increasing the functionality of LSIs by integrating various kinds of materials and devices on them has been increasing. In order to solve these problems and satisfy new requirements, it is essential to new hetero-integration technologies by merging different kinds of technologies with LSI technology. In this research project, we aim to realize a new integrated optoelectronic system-on-a chip with high performance, low power consumption and high functionality by merging three-dimensional integration technology and optoelectronic integration technology.

【Research Methods】

In this project, we aim to realize three-dimensionally stacked opto-electronic system-on- a chip as shown in Fig.1. The key to achieve such system is a new integration technology to bond different kinds of chips and devices such as photonic devices on LSI chips with high alignment accuracy. We develop a new grapho-assembly technology as a key technology to achieve high alignment accuracy in integrating different kinds of chips and devices on LSI chips. Different kinds of chips such as LSIs, photonics and MEMS are self-assembled onto a substrate by making use of surface tension of liquid in a grapho-assembly technology. We dramatically improve the alignment accuracy in the self-assembly by independently controlling the volume and the surface area of liquid droplets on the chip and the substrate by nano-structures formed on them. The other key technology is the optical interconnection and the silicon photonics. We investigate the possibilities of vertical optical interconnection called through-silicon photonic via (TSFV) together with silicon photonic devices.

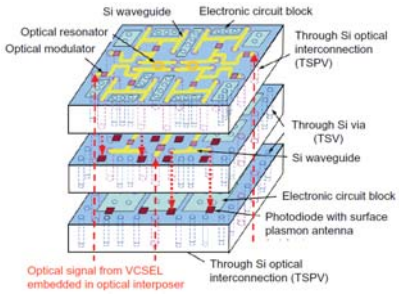

Fig. 1 Configuration of 3-D stacked optoelectronic system -on- a chip.

【Expected Research Achievements and Scientific Significance】

It becomes possible to three-dimensionally integrate different kinds of chips with high alignment accuracy of 50nm to 100nm by using the grapho-assembly technology. As a result, we can realize a three-dimensionally stacked opto-electronic system-on-a chip for the first time where three-dimensional integration technology and the optical interconnection and silicon photonics technology. Many stacked chips are vertically connected by high density of TSVs (more than 100 million TSVs/cm^2). Stacked chips are also connected by vertical optical interconnection (TSFV). In addition, it is expected that researches in a new area of integrated optoelectronic devices and systems are accelerated by the research achievements of this project. Furthermore, this project will contribute to the progresses in LSI technology, green IT technology and computer technology.

【Publications Relevant to the Project】

・T. Fukushima, M. Koyanagi et al. “New Heterogeneous Multi-Chip Module Integ- ration Technology Using Self-Assembly Method”, IEEE International Electron Devices Meeting Tech. Dig., pp.499-502, 2008.

・M. Koyanagi, et al. “Three-Dimensional Integration Technology Based on Wafer Bonding with Vertical Buried Interconnections”, IEEE Trans. on Electron Devices, Vol.53, pp.2799-2808, 2006.

【Term of Project】 FY2009-2013

【Budget Allocation】 163,100 Thousand Yen

【 Homepage Address and Other Contact Information】

http:// www.sd.mech.tohoku.ac.jp