（様式４）

二国間交流事業 共同研究報告書

令和 6 年 1 月 30 日

独立行政法人日本学術振興会理事長 殿

［日本側代表者所属機関・部局］
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1. 事 業 名 相手国: 中国 (振興会対応機関: NSFC)との共同研究

2. 研究課題名

（和文） 耐放射線記憶素子の設計とテストに関する研究

（英文） Research on Design and Test for Radiation-Hardened Storage-Cells

3. 共同研究実施期間 2021 年 4 月 1 日 ～ 2023 年 12 月 31 日 (共同研究:2 年 9 ヶ月)

【延長前】 年 月 日 ～ 年 月 日 (年 ヶ月)

4. 相手国側代表者(所属機関名・職名・氏名【全て英文】)

Anhui University・Associate Professor・YAN, Aibin

5. 委託費総額(返還額を除く)

本事業により執行した委託費総額		3,513,474 円
内訳	1年度目執行経費	1,366,100 円
	2年度目執行経費	1,366,100 円
	3年度目執行経費	781,274 円

6. 共同研究実施期間を通じた参加者数(代表者を含む)

日本側参加者等	8 名
相手国側参加者等	7 名

＊ 参加者リスト(様式 B1(1))に表示される合計数を転記してください(途中で不参加となった方も含め、全ての期間で参加した通算の参加者数となります)。

7. 派遣・受入実績

	派遣		受入
	相手国	第三国	
1 年度目	0	0	0 (0)
2 年度目	0	0	0 (0)
3 年度目	2	1	0 (0)

＊ 派遣・受入実績(様式 B1(3))に表示される合計数を転記してください。

派遣:委託費を使用した日本側参加者等の相手国及び相手国以外への渡航実績(延べ人数)。

受入:相手国側参加者等の来日実績(延べ人数)。カッコ内は委託費で滞在費等を負担した内数。

8. 研究交流の概要・成果等

(1)研究交流概要(全期間を通じた研究交流の目的・実施状況)

Research Purpose

In integrated circuits (LSIs) used in critical fields such as aerospace, data centers, autonomous driving, robots, and medical care, soft errors caused by neutron rays from space have become serious. Therefore, the development of soft-error-resistant logic storage devices (latch, flip-flop) is indispensable.

First problem: In previous research, soft errors due to direct radiation hits to multiple nodes in the same element could not be effectively avoided, resulting in insufficient multi-node soft error tolerance.

Second problem: Soft-error-resistant logic storage devices also hide other problems such as structural defects introduced during production. Standard LSI post-manufacturing testing becomes less effective and serious reliability issues may be missed.

In this joint research, we focused on the necessity and urgency of simultaneous solution of the above fundamental problems.

Research Implementation

Due to COVID-19 related travel restrictions during large parts of this project, most meetings have been conducted online via Zoom and via email. To ensure the best chance of success for this project, budget originally allocated for travel has been used to purchase infrastructure (online collaboration server, cameras, etc.) for more efficient online meetings and remote collaboration work.

Secondly, the sudden hospitalization and subsequent passing of Prof. Kajihara impacted not only the latter phase of this project but was also a major loss for the whole research community.

Despite these unforeseen challenges, the research has been implemented smoothly and major academic contributions have been made towards solving the research goals introduced above.

In 2023, Prof. Aibin Yan moved from Anhui University to Hefei University of Technology, and after the lifting of travel restrictions in Oct. 2023, a joint workshop organized at Hefei University of Technology brought our research groups closer together.

(2)学術的価値(本研究交流により得られた新たな知見や概念の展開等、学術的成果)

This joint research has a high degree of originality of simultaneous realization of high reliability and high quality. Overall, **7 journal articles, 12 conference papers**, and 1 workshop contributions/posters have been published. Among the conference papers, **one received a Best-Paper Award**.

Summary of key results from this project:

- Members of the Kyutech group (Prof. Wen, Prof. Holst) published a prospective study on a simulation approach to quantify error tolerance of AI accelerators [1]. This simulation technique also supports soft errors and can be used to **investigate soft-error tolerant storage elements in context of real-world applications**. The paper published at the IEEE Asian Test Symposium 2021 has been awarded ***"Best Paper of ATS21"***.

- **A new fault model has been developed** that shows, how soft-errors influence the internal circuitry of storage elements that also contain permanent production defects (WP1). Based on this new fault model, extensive SPICE simulations have been carried out to estimate soft-error tolerance and testability of storage elements (WP2) and **an improved test-aware hardened latch design was developed**. The results have been published in IEICE Transactions on Information and Systems [2].

- A new built-in self-testable soft-error-hardened scan-cell was developed. This new method enables for the first time **in-field testing for a hardened latch structure** (WP3). In-field testing is essential to mitigate early-life failures (ELF) due to accelerated aging coming from process variations that cannot be detected right after manufacturing. The new structure was simulated in SPICE modeling both permanent defects and

soft errors (WP2). The results of this research have been published in the proceedings of the IEEE European Test Symposium (ETS) [3].

- Various new and innovative **Double-Node-Upset tolerant storage element designs** were proposed. Among them a high-performance CMOS latch [4], a low-power flip-flop [5], and various cross-coupled SRAM cells [6, 7]. All these results were published at international conferences and as journal papers.

- Finally, ultra-reliable latch designs that can **tolerate even Triple-Node-Upsets** [8] and **Quadruple-Node-Upsets** [9] have been published at the Asian Test Symposium 2023 and ITC Asia 2022, respectively, pushing the boundaries of robust design methods even further.

[1] **S. Holst**, L. Bumun, and **X. Wen**, "GPU-Accelerated Timing Simulation of Systolic-Array-Based AI Accelerators" in Proc. IEEE Asian Test Symposium (ATS), Nov. 2021, pp. 127-132. (***Best Paper***)

[2] R. Ma, **S. Holst**, **X. Wen**, Aibin Yan, and Hui Xu: "Evaluation and Test of Production Defects in Hardened Latches," IEICE Transactions on Information and Systems, Vol. E105-D, No. 5, May 2022.

[3] **S. Holst**, R. Ma, **X. Wen**, A. Yan, Hui Xu: "BiSTAHL: A Built-In Self-Testable Soft-Error-Hardened Scan-Cell," in Proc. IEEE European Test Symposium (ETS), May 2023.

[4] A. Yan, K. Qian, T. Song, Z. Huang, T. Ni, Y. Chen, and **X. Wen**: "A Double-Node-Upset Completely Tolerant CMOS Latch Design with Extremely Low Cost for High-Performance Applications" Integration, the VLSI Journal, Vol. 86, pp. 22-29, Apr. 2022

[5] A. Yan, Y. He, Z. Li, J. Cui, T. Ni, Z. Huang, P. Girard, and **X. Wen**, "A Highly Robust and Low Power Flip-Flop Cell with Complete Double-Node-Upset Tolerance for Aerospace Applications" IEEE Design & Test, Vol. 40, No. 4, pp. 34-41, Aug. 2023.

[6] A. Yan, J. Xiang, A. Cao, Z. He, J. Cui, T. Ni, Z. Huang, **X. Wen**, and P. Girard: "Quadruple and Sextuple Cross-Coupled SRAM Cell Designs with Optimized Overhead for Reliable Applications" Trans. on Device and Materials Reliability, Vol. 22, No. 2, pp. 282-295, Jun. 2022

[7] A. Yan, J. Xiang, Z. Huang, T. Ni, J. Cui, P. Girard, and **X. Wen**, "Two Sextuple Cross-Coupled SRAM Cells with Double-Node-Upset Protection and Cost Optimization for Aerospace Applications" Microelectronics Journal, Vol. 139, 105908, Sep. 2023.

[8] Yan, X. Li, Z. Zhou, Z. Huang, T. Ni, and **X. Wen**, "Advanced DICE Based Triple-Node-Upset Recovery Latch with Optimized Overhead for Space Applications" Proc. of IEEE Asian Test Symp., Paper 2A-1, Beijing, China, Oct. 2023.

[9] A. Yan, S. Song, J. Zhang, J. Cui, Z. Huang, T. Ni, **X. Wen**, and P. Girard: "Cost-Optimized and Robust Latch Hardened against Quadruple Node Upsets for Nanoscale CMOS" in Proc. of IEEE Int'l Test Conf. in Asia, Paper A4-2, Taipei, Taiwan, Aug. 2022.

(3)相手国との交流(両国の研究者が協力して学術交流することによって得られた成果)

Due to ongoing COVID-19 related travel restrictions in the first years of this project, all meetings have initially been conducted online via Zoom and collaboration also continues via email. To ensure the best chance of success for this project, budget originally allocated for travel has been used to purchase infrastructure (online collaboration server, cameras, etc.) for more efficient online meetings and remote collaboration work.
Despite these difficulties, numerous joint papers have been prepared and subsequently published during that time.
Travel and in-person meetings became possible again in 2023 after lifting of the travel restrictions. A delegation from Japan (Prof. Wen, Prof. Holst) visited China in October 2023 for one week. The travel included the participation at the IEEE Asian Test Symposium 2023 in Beijing, followed by the participation at the "CCF TCFTC@U & China-Japan Bilateral International Workshop on Dependable Integrated Circuits" organized by Prof. Yan in Hefei. **Prof. Wen gave an opening keynote** at the IEEE Asian Test Symposium 2023 and **Prof. Holst gave an invited half-day tutorial** on "Test and Health Monitoring under Approximations and Variations" together with Prof. Hans-Joachim Wunderlich (retired, formerly University of Stuttgart). Project partners from China participated in both events. **Prof. Wen and Prof. Holst both gave talks during the full-day "CCF TCFTC@U & China-Japan Bilateral International Workshop on Dependable Integrated Circuits"** at Hefei Institute of Technology (HFUT). This workshop was organized by Prof. Yan and visited by students and faculty of HFUT, Anhui University of Science and Technology, Anhui University, Hunan University, and Japanese delegations

from Ehime University and Tokushima University.

(4)社会的貢献（社会の基盤となる文化の継承と発展、社会生活の質の改善、現代的諸問題の克服と解決に資する等の社会的貢献はどのようにあったか）

Advanced VLSI technology enables ubiquitous communications, advanced automation and autonomy, as well as discoveries in basic research essential for advancement of human society. This project addressed one of the main reliability threats to advanced VLSI technology, namely erroneous calculations that originate from background radiation striking the small transistors and causing upsets.
The new data produced by this project and the advancements to radiation-tolerant storage cell designs provide a strong foundation for a safe and secure VLSI technology enabling autonomous systems at land, in the air as well as in space.

(5)若手研究者養成への貢献（若手研究者養成への取組、成果）

Various bachelor and master students were working on topics related to this project, helping them getting real-world research experience using current and future VLSI technology. In particular, two Kyutech students were impacted very positively by working on project topics:

- **Lim Bumun** (Korean): Lim was working on the prospective study of "GPU-Accelerated Timing Simulation of Systolic-Array-Based AI Accelerators", he co-authored the ATS 2021 paper that subsequently received the best-paper award. This research helped him greatly **graduating his Master-course with distinction** and getting hired by an internationally operating Japanese company.

- **Ruijun Ma** (Chinese): Ma joined Kyutech as a Ph.D. student just before the start of this project. He was instrumental in this project and co-authored several papers. During this project, **Ma completed his Ph.D. study with the topic "Defects in Hardened Latches: Analysis, Detection, and Evaluation"** in 2022. This project helped him achieving a position at Anhui University of Science and Technology where he is currently continuing his research on radiation-hardened design.

(6)将来発展可能性（本事業を実施したことにより、今後どの様な発展の可能性が認められるか）

The results of this project provide a strong foundation for numerous further developments.
- Both, testable single-node-upset tolerant storage elements, and multi-node-upset tolerant storage elements have been developed in this project. A further study may investigate **testable multi-node-upset tolerant storage elements** by combining the various concepts developed in this project.
- The developed testable storage element designs can be extended for **online monitoring of upsets and aging**. This would enable new ways of silicon lifecycle management that include early degradation warnings and fail-safe operations.
- Further studies may explore physical implementation and **post-silicon validation** of the developed storage cells. This is a natural step toward industrial adoption, but it requires a much larger funding than what is possible in the framework of this project.

(7)その他（上記(2)～(6)以外に得られた成果があれば記載してください）
例：大学間協定の締結、他事業への展開、受賞など

The research in this project sparked interest from European universities and companies in possible applications of the developed cells for temper-proofing high-security devices such as smart-cards. In general, there has been considerable interest in possible monitoring solutions in conjunction with silicon lifecycle management. Concrete agreements are not yet finalized.