【Grant-in-Aid for Specially Promoted Research】
Science and Engineering (Engineering)

Title of Project : Design of Electronic Properties and Development of High-Mobility Channel Technology for Low Power/High-Speed Nano-CMOS Devices

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Research Area : Applied physics, Thin film/Surface and interfacial physical properties

Keyword : Thin film, Interface, Semiconductor, Epitaxial growth

【Purpose and Background of the Research】

In Si ultra-large scale integrated circuit (ULSI) devices, the improvement of current drivability is essential for lowering the power consumption and increasing the speed. The strained-channel technology to obtain higher carrier mobility than bulk Si has already been introduced into ULSI devices in order to overcome the physical properties of Si. This mobility enhancement of Si using strain has also a limit and it is indispensable for future nano-scale ULSIs to introduce new materials, which have much higher carrier mobility than strained Si, into the channel region of metal-oxide-semiconductor (MOS) transistors.

In this research project, we focus on the design of electronic properties of Ge using strain and Sn addition and the development of new channel technology using Ge-related materials, aiming to establish the high-mobility channel technology for future nano-scale complimentary-MOS (CMOS) devices.

【Research Methods】

It is possible to obtain the high mobility both electrons and holes compared with strained Si by adding the strain of about 1% to Ge. Furthermore, the addition of strain over 1% and 20% Sn into Ge induce the change in the electronic band structures from an indirect- to direct-transition type and hence the electron and hole mobility has been expected to be drastically enhanced.

We will establish the epitaxial growth technology to fabricate the strained-Ge/GeSn/Si heterostructure, examine the electronic and electrical properties of strained Ge and GeSn, and also propose the technology for controlling the MOS interface properties. (Fig. 1)

【Expected Research Achievements and Scientific Significance】

The Sn addition in Ge brings new functionality and flexibility into Group IV semiconductor materials. One of important points is that both n- and p-MOS transistors in future nano-scale CMOS devices are achievable using Ge-related materials having high compatibility with Si processes. This technology has a potential that the trend of future ULSI technology can be revolutionized and, therefore, the industrial impact is extremely large.

In addition, because these materials with a large strain and a high Sn content are theoretically expected to have a direct band gap, the application for solar cells, optical devices and so forth will be developed.

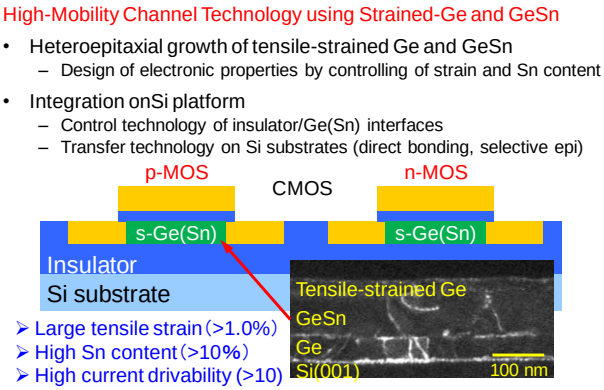

Fig. 1 Content of this research project

【Publications Relevant to the Project】

[1] Y. Shimura, N. Tsutsui, O. Nakatsuka, A. Sakai and S. Zaima, "Control of Sn Precipitation and Strain Relaxation in Compositionally Step-Graded $Ge_{1-x}Sn_x$ Buffer Layers for Tensile-Strained Ge Layers", Jpn. J. Appl. Phys., **48**, 04C130-1-4 (2009).

[2] S. Takeuchi, Y. Shimura, O. Nakatsuka, S. Zaima, M. Ogawa and A. Sakai, "Growth of Highly Strain-Relaxed $Ge_{1-x}Sn_x$/Virtual-Ge by a Sn Precipitation Controlled Compositionally Step-Graded Method", Appl. Phys. Lett., **92**, 231916 (2008).

【Term of Project】 FY2010-2013

【Budget Allocation】 344, 600 Thousand Yen

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