【Grant-in-Aid for Specially Promoted Research】
Science and Engineering (Engineering)

Title of Project : Study on fabrication process of 3-D structured MOS transistor having atomically flat gate insulator/Si interface

Tadahiro Ohmi
(Tohoku University, New Industry Creation Hatchery Center, Professor)

Research Area : Electronic materials, Electric materials

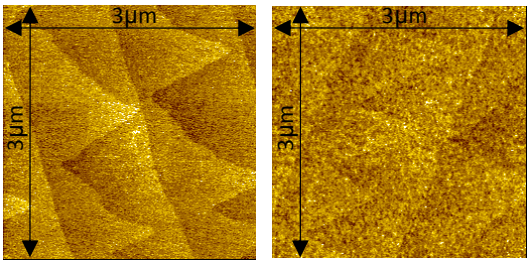
Keyword : Electrical and electronic materials (semiconductor)

【Purpose and Background of the Research】

The current semiconductor technology can fabricate LSI only on (100) Si surface using 2-D planar structure transistors. Thus, the current silicon technologies are now facing with very severe standstill, and the progress of speed performance of the silicon LSI has completely stopped. In order to overcome these troubles, it is required to create the process technologies for manufacturing the three-dimensional structure MOS transistors, which have the atomically flat interface between the gate insulator film and the silicon substrate, on any crystal orientation silicon surface. The research objective of this project is to create the balanced CMOS silicon LSI having a very excellent speed performance and very low power consumption. Therefore, it is essentially required to develop the flattening technologies for the any crystal orientation silicon surface and silicon sidewall surface of the 3-D MOS transistors.

【Research Methods】

The performance of the silicon LSIs is drastically improved by introducing the following three technologies, (1)Accumulation Mode MOS transistor instead of conventional Inversion Mode MOS transistors, (2)3-D structure on (551) orientation SOI wafer instead of 2-D planer structure on (100) orientation wafer, (3)atomically flat interface between the gate insulator film and silicon substrate. However, these technologies cannot be realized by using the current silicon technologies. Only by making good use of the new manufacturing system based on the ultra clean technologies and the radical reaction processes, these three technologies can be realized. Figure 1 shows the AFM images of SiO_2/Si interface fabricated by radical oxidation and thermal oxidation on the atomically flat Si(100) surface. The SiO_2/Si interface fabricated by radical oxidation is maintained the mono atomic layer step and the atomically flat terrace, although, that by thermal oxidation is roughened. In this project, we develop the flattening technologies for the Si surface and Si sidewall surface of the 3-D structure by making good use of the radical reaction based new manufacturing technologies by using the damages free plasma equipments which we have developed.



Radical SiO_2/Si　　Thermal SiO_2/Si

Fig. 1 AFM images of SiO_2/Si interface

【Expected Research Achievements and Scientific Significance】

By achieving this project, the speed performance of MOS transistors is drastically improved, and the variability of transistor characteristic and 1/f noise are drastically reduced. As the results, the power consumption is lowered with maintaining the reliability. Thus, the realization of the ultra high performance information and communication device with very low power consumption is of great scientific significance.

【Publications Relevant to the Project】

1. R. Kuroda, T. Ohmi, et al., IEEE Trans. Electron Dev., VOL.56, NO.2, pp.291-298, February 2009.
2. T. Ohmi, et al., IEEE Trans. Electron Dev., VOL.54, NO.6, pp.1471-1477, June 2007.

【Term of Project】 FY2010-2014

【Budget Allocation】 474, 400 Thousand Yen

【 Homepage Address and Other Contact Information】

http://www.fff.niche.tohoku.ac.jp/
Email: ohmi@fff.niche.tohoku.ac.jp