【Grant-in-Aid for Scientific Research (S)】
Science and Engineering (Engineering)

Title of Project : Precise structure control of 3-dimensional integration CMOS using high mobility materials through layer transfer

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Research Area : Electric and Electronic Material Engineering
Keyword : MOSFET, Germanium, III-V compound semiconductors

【Purpose and Background of the Research】

The physical limitations of miniaturization of CMOS used in LSI have recently more evident, leading to the difficulty in satisfying both increase in transistor numbers and improvement in performance. From this viewpoint, 3-dimensional stacked CMOS has started to be examined to increase the number of CMOS without losing the performance. In this study, we establish following science and technologies needed for realizing 3D stacked CMOS using high mobility channel materials, which is promising as a future scaled CMOS, (1) channel formation by layer transfer (2) SD formation and 3D connectivity technology (3) MOS interface control. A typical example of the CMOS structures is shown in Fig. 1. We pursue for methodology of precisely controlling the structure down to nm order, resulting in realizing performance of 3D stacked CMOS and clarifying the direction for future generation scaled CMOS.

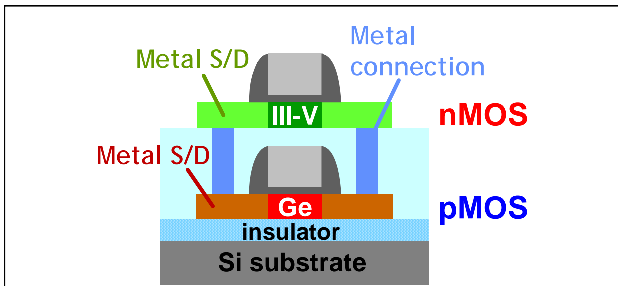

Fig.1 example of stacked CMOS structure

【Research Methods】

(1) Channel formation by layer transfer

We realize ultrathin and flat GOI/III-V-OI films with high crystal quality by using smart cut, shown in Fig. 2, epitaxial lift-off and so on. In addition, we clarify the electronic properties of ultrathin semiconductor channels.

(2) Low temperature source/drain (S/D) formation and 3D connectivity

We pursue for metal S/D materials and the formation process appropriate for the ultrathin Ge/III-V channels with high controllability at low temperature.

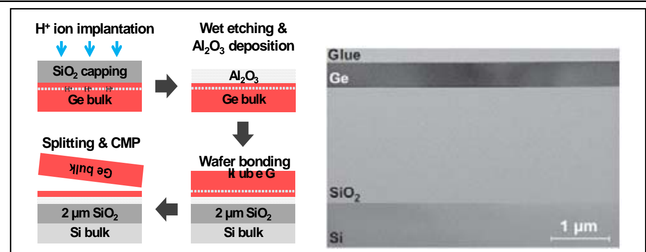

Fig. 2 GOI formation method by smart cut and example of fabricated GOI structure

(3) High quality MOS interface formation

We establish MOS interface control technologies for minimizing GOI/III-V-OI MOS interface defects.

【Expected Research Achievements and Scientific Significance】

・Establish formation and control technologies for realizing 3D integrated III-V/Ge CMOS with understanding the basic physics

・Clarify interface physics underlying nm-size contacts at hetero-material interfaces

・Develop the transfer technologies of different materials and expand the applications

・Esbatlish comprehensive understanding of the III-V/Ge CMOS technologies from fandamental science to device design and manufacturing.

【Publications Relevant to the Project】

・S. Takagi et al., "III-V/Ge Channel MOS Device Technologies in Nano CMOS era", Jpn. J. Appl. Phys., vol. 54, 06FA01 (2015)

・T. Irisawa, T. Maeda et al., "Demonstration of Ultimate CMOS based on 3D Stacked InGaAs-OI/SGOI Wire Channel MOSFETs with Independent Back Gate", 2014 Symposium on VLSI Technology, 146 (2014)

【Term of Project】 FY2017-2021

【Budget Allocation】 158,900 Thousand Yen

【Homepage Address and Other Contact Information】

http: // www.mosfet.k.u-tokyo.ac.jp/