【Grant-in-Aid for Scientific Research (S)】

Integrated Disciplines (Informatics)

Title of Project : Basic Research of a Dark-Silicon-Based Logic-LSI Technology for Brainware Computing

Takahiro Hanyu
(Tohoku University, Research Institute of Electrical Communication, Professor)

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Research Area : Information Science
Keyword : Computer Systems

【Purpose and Background of the Research】

We study on dark-silicon logic-LSI technology for brainware (brain-inspired) computing. The brainware computing that mimics the human-brain function has a possibility to realize ultra-low power computation for real-time objection recognitions. In order to realize the brainware computing in LSI, extremely fine-grain power gating (EFGPG) techniques are required, where the EFGPG techniques allow LSIs to consume power only on circuits operated.

In this study, we focus on asynchronous control essentially used in the human-brain information processing and exploit it with the dark-silicon approach. Hence, we research and develop asynchronous circuits with EFGPG techniques for real-time brainware computing.

【Research Methods】

We develop the dark-silicon asynchronous logic LSI technologies that can control the gate-level power gating. To verify the functionality of the dark-silicon asynchronous logic LSI in a fabricated chip, we study three main topics as follows:

1) FY2016-2017
Dark-silicon asynchronous basic logic blocks are designed for small-scale circuits. In addition, equivalent CMOS integrated circuits are designed and fabricated to verify the basic function.
2) FY2017-2018
Hybrid CMOS/Magnetic tunnel junction (MTJ)-based dark-silicon asynchronous logic circuits are designed and fabricated to verify the gate-level power gating for brainware computing.
3) FY2018-2020
Based on the experimental results from the CMOS/MTJ hybrid chip, a low-level vision chip based on the dark-silicon asynchronous logic gates are designed and evaluated for real-time brainware computing.

【Expected Research Achievements and Scientific Significance】

To the best our knowledge, it is the first research to combine asynchronous-circuit technologies and MTJ-based gate-level power gating techniques for ultra-low power computation in both domestic and overseas.

The asynchronous circuits exhibit an intrinsic function that autonomously detects circuit operations using local signals. We exploit the function to reduce unnecessary power consumption wasted as much as possible for ultra-low power computation. In addition, using the MTJ-based nonvolatile devices, the gate-level power gating can be applied to the whole chip because of the nonvolatility.

For applications other than brainware computing, the proposed dark-silicon logic-LSI techniques can be used for Internet-of-Things (IoT) devices consisting of sensors and integrated circuits. As the number of IoT devices is expected to be 80 billions in 2025, the proposed ultra-low power technique would be a key technology in future computing systems.

【Publications Relevant to the Project】

T. Hanyu, et al., “Spintronics-Based Nonvolatile Logic-in-Memory Architecture Towards an Ultra-Low-Power and Highly Reliable VLSI Computing Paradigm,” *Proc. 2015 DATE Conference*, pp. 1006-1011, Mar. 2015 (invited).

T. Hanyu, et al., “Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing,” *Proc. of the IEEE*, 2016 (to appear).

【Term of Project】 FY2016-2020

【Budget Allocation】 127,100 Thousand Yen

【Homepage Address and Other Contact Information】

http://www.ngc.riec.tohoku.ac.jp
hanyu@riec.tohoku.ac.jp