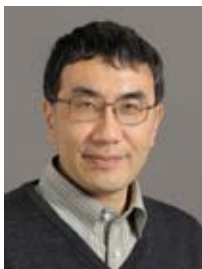


## 【Grant-in-Aid for Scientific Research(S)】

### Integrated Disciplines (Informatics)



Title of Project : A Study on Building-Block Computing Systems using Inductive Coupling Interconnect

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( Keio University, Faculty of Science and Technology, Professor )

Research Area : Informatics

Keyword : Computer Architecture

#### 【Purpose and Background of the Research】

Building-Block Computing systems enable to build an appropriate system for the target application just by selecting required chips: CPU, memory modules and accelerators and stacking them. Inductive coupling interconnect between chips form a network –on-chip automatically, and a system is optimized even if the specification is not fixed beforehand. For realizing such systems, inter-chip wireless inductive coupling techniques, self-organized network-on-chips, fault tolerant architectures, optimized power control, and a flexible operating system with virtualization facilities are investigated.

#### 【Research Methods】

For establishment of building-block computing systems, crosscutting researches on circuit, architectures and system software are required. The followings will be investigated in each research field: (1) Although a number of research trials have been reported, the standard design flow of inductive coupling has not been established. Our first goal is developing an IP (Intellectual Property) of inductive coupling interconnect for easy use of the technology. In order to reduce the footprint of inductors, digital circuits must be implemented inside the inductors. Power supply using inductive coupling link is also our challenge. (2) Self-organized network-on-chip which can be formed just by stacking chips will be investigated. (3) Techniques on fault tolerant self optimizing architectures are important to form building-block systems. (4) Power control is essential in 3D chip stacking, since the heat dissipation is difficult. We will use integrated power control techniques from the system software to circuits. (5) A flexible operating system with virtualization technique is needed to integrate all chips into a system.

We will develop the first prototype multi-core system using inductive coupling in 2013. Based on the prototype, techniques on each layer will be investigated. In 2016, we will develop a final system in which various chips can be stacked as shown in Figure 1, and demonstrate our techniques on it.

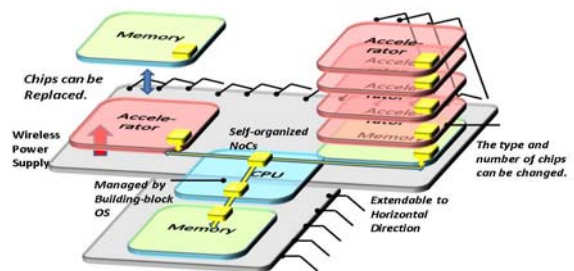


Figure 1 The final prototype

#### 【Expected Research Achievements and Scientific Significance】

Building block computing systems can solve problems on recent advanced semiconductor technologies: I/O problems and expanding cost to develop a large chip. It can be applied wide area of embedded systems including sensor networks for cyber physical space and car electronics. The lifetime of the product will be stretched by replacing chips. It also contributes the reuse of the chips and so save the earth resource.

#### 【Publications Relevant to the Project】

- 3-D NoC Inductive Coupling Links for Building Block SoCs,” Yasuhiro Take, Hiroki Matsutani, Daisuke Sasaki, Michihiro Koibuchi, Tadahiro Kuroda, Hideharu Amano, IEEE Trans. on Computers, (In press)
- N. Miura, T. Shidei, Y. Yuan, S. Kawai, K. Takatsu, Y. Kiyota, Y. Asano, and T. Kuroda, “A 0.55V 10fJ/bit Inductive-Coupling Data Link and 0.7V 135fJ/Cycle Clock Link with Dual-Coil Transmission Scheme,” IEEE JSSC, vol.46, no.4, pp.965-973, Apr. 2011

【Term of Project】 FY2013-2017

【Budget Allocation】 166,400 Thousand Yen

#### 【Homepage Address and Other Contact Information】

[http://www.am.ics.keio.ac.jp/kaken\\_s](http://www.am.ics.keio.ac.jp/kaken_s)