【Grant-in-Aid for Scientific Research(S)】
Science and Engineering (Engineering Ⅰ)

Title of Project : Study on Sub-μW Microprocessors using Adiabatic Single-Flux-Quantum Circuits

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Research Area : Electronics devices and systems

Keyword : Electronics devices, integrated circuits

【Purpose and Background of the Research】

Single-flux-quantum (SFQ) circuits, which utilize quantized flux in a superconducting loop as logical bit information, can operate at very high speed beyond 100 GHz clock frequencies with extremely low power consumption. Many studies are under way around the world to realize high-end digital systems.

The purpose of this project is to verify the utmost limit of low power operations of SFQ circuits. We bring in new principles and technologies to reduce the power consumption of the SFQ circuits, which include new operation principles of SFQ logic gates, such as adiabatic SFQ circuits, new circuit architectures and new process technologies. Our goal is to reduce the power consumption of the SFQ circuits to 1/400 – $1/10^5$ of current SFQ circuits. In the end of the project, we will demonstrate a 16b SFQ microprocessor operating with 50 μW power consumption. We will also establish the fundamental technologies for sub-μW microprocessors, which are truly-unexplored regions in the digital electronics world.

【Research Methods】

In order to reduce the power consumption of SFQ circuits, we propose new operation principles, such as adiabatic operations of the SFQ circuits and a new circuit structure for low bit-error-rate SFQ circuits. In addition, we will investigate an inductive-load-biasing technique, a gate-to-gate passive-transmission-line technology, sub-μm junction process to reduce the critical currents, and asynchronous circuit design approaches.

Figure 1 shows a proposed adiabatic SFQ gate, whose circuit structure is known as a quantum flux parametron (QFP) but its operation principle is different from the QFP. By removing the hysteretic behavior in its switching events and operating it adiabatically, the switching energy will be reduced to the order of the thermal energy (~k_BT) in principle.

【Expected Research Achievements and Scientific Significance】

The performance of present integrated circuits is mainly limited by their power consumption nowadays. Proposed low-power SFQ integrated circuits will achieve more than six orders of magnitude reduction of the power consumption of the chip, resulting in the overwhelming power reduction of high-end computing systems even if the power of cryocooler is included.

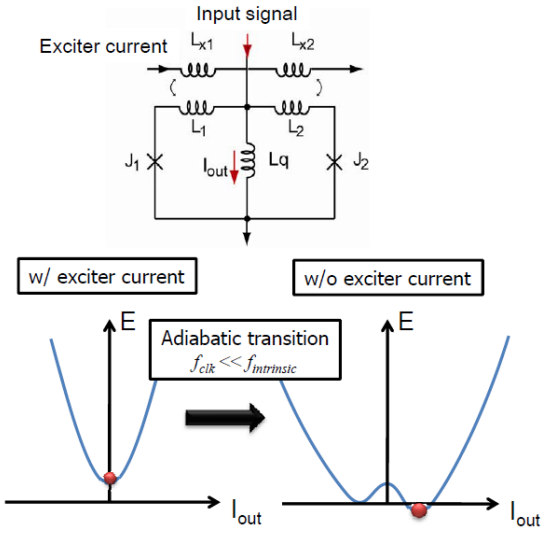

Fig. 1 Operation principle of adiabatic SFQ logic circuits

【Publications Relevant to the Project】

・H. Park, *et. al.*, "Design and Implementation of SFQ Half-Precision Floating-Point Adders," IEEE Trans. Appl. Supercond., vol. 19, pp. 634-639, 2009.
・T. Nishigai, S. Yamada, N. Yoshikawa, "Design and implementation of low-power SFQ circuits using LR-load biasing technique," Physica C, vol. 445-448, pp. 1029-1033, 2006.

【Term of Project】 FY2010-2014

【Budget Allocation】 163,300 Thousand Yen

【Homepage Address and Other Contact Information】

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