

Nano-scale Structural Control of Cu interconnects Using An Extreme High-purity Electro-plating Process and Its Application to Next Generation Nano-scale ULSI

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【Outline of survey】

The purpose of this study is to develop an innovative technological process which yields a substantial decrease in the resistivity of Cu interconnects of less than 28nm to prevent ULSI from performance degradation. The Cu interconnects consist of both an inner conductive Cu and its outer high-resistivity barrier metal. However, lowering of resistivity by reducing the thickness of the high-resistivity barrier metal has been investigated intensively, the resistivity reduction process of inner Cu itself has not received much consideration. We have focused our attention on the purification of the Cu interconnects and investigating the forming process using a high-purity nominal 9N-Cu anode and nominal 6N-CuSO₄ · 5H₂O electrolyte. By utilizing a high-purity process, we have created 50nm wide Cu interconnects with grain sizes about 10% larger and with 20% lower resistivity than those made by the conventional process. Above results imply that a high-purity plating process could be a key technology for the reduction of the resistivity of Cu interconnects.

In this study, we investigate the development of the ultra-high-purity Cu anode and CuSO₄ · 5H₂O electrolyte about 2 orders of purity higher compared to high-purity commercial processes and also forming Cu interconnects without additives which might introduce impurities into Cu during plating. In addition, we also investigate barrier metal free process using insulator films of low-dielectric constant with barrier properties.

Our research goal is to realize the foundations of a new process for the multi-level Cu interconnect system with an innovative high-conductivity on the basis of the new technologies discussed above.

【Expected results】

The newly developed process is considered to have excellent compatibility with the LSI process, because low resistivity Cu interconnects can be obtained by only replacing conventional anodes and CuSO₄ · 5H₂O electrolytes with ultra-high-purity ones and by removing additives from electrolyte. The process developed for the realization of an innovative low resistivity Cu interconnect will contribute to the advance of Japanese LSI manufacturing industries and creation of a new electronic and information industry with low electric consumption. This is indispensable for the preservation of global environment.

【References by the principal investigator】

- S.Tashiro, K.P.Khoo, T.Nagano, J.Onuki, Y.Chonan, H.Akahoshi, T.Tobita, M.Chiba, K.Ishikawa and N.Ishikawa, "The Development of an Innovative Process of Large-Grained and Low Resistivity CuWires for less than hp45nm ULSI", In Proc.International Interconnect Technology Conference, pp.46-48, June 2007.
- Jae-Won Lim, K.Mimira and M.Isshiki, "Precise impurity analysis of Cu film by GDMS", Appl. Phys.A80, 1105-1107, 2005.

【Term of project】 FY2008—2012

【Budget allocation】

161,300,000 yen (direct cost)

【Homepage address】

None