Principal Researcher	Mitsumasa Koyanagi	Number of Reserchers	6
Research Institution Department Title	Professor, Bioengineering and Robotics, Tohoku University	Location of Institution	Sendai
Title of Project	High Performance Parallel Processor System Using Three-Dimensional Processor Chips.		

Abstract of Research Project	The purpose of this research project is to develop a new three-dimensional (3D) processor chip and a high performance parallel processor system with 3D processor chips which are indispensable in a multimedia society. High system performance can not be expected in parallel processor systems with common buses due to the bus bottleneck problem. Then, we propose a new parallel processor system with 3D multi-port memory chips and 3D processor chips which are connected by the optical interconnection. 3D multi-port memory acts as a shared memory with multi-ports. Optical interconnection is used as a broadcast bus. We also realize a new 3D processor chip with 3D multi-port memory input by stacking 3D multi-port memory chip on a processor chip. We construct a test module for parallel processor system where 3D processor chips and 3D multi-port memory chips are connected by optical interconnection. In this system, data sharing is performed among several 3D multi-port memory chips and several 3D processor chips through the optical interconnection.

References	1) T. Ono, H. Kurino and M. Koyanagi et al., Three-Dimensional Processor System Fabricated by Wafer Stacking Technology, Proceedings of International Symposium on Low-Power and High-Speed Chips (COOL Chips V), , 186 - 193 (2002) 2) H. Kurino, Y. Nakagawa, M. Koyanagi et al., Biologically Inspired Vision Chip with Three Dimensional Structure, IEICE Transactions on Electronics, E84-C (12), 1717 - 1722 (2001)

Term of Project	Fiscal years 2003-2007 .　(5years)					
Budget	FY2003	FY2004	FY2005	FY2006	FY2007	TOTAL
Allocation (in thousand of yen)	29,000	23,800	17,200	14,200	3,900	88,100
Homepage Address		http://www.sd.mech.tohoku.ac.jp				