

Design and Fabrication of Printed Organic Thin-Film Transistors on a Flexible Substrate

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The development of organic thin-film transistors (OTFTs) for use as a switching and driving device in flexible displays, low-cost printed electronics, and printed electromechanical systems (PEMS) is a very important field of study because of the increasing demand for such devices. Consequently, many of the early demonstrations of OTFTs and circuits made use of a variety of conventional device fabrication techniques for material deposition and patterning, including vapor-phase deposition, photolithography, and wet and dry etching. However, these methods have disadvantages: they often require photoresists, solvents, and developers that are incompatible with the materials that must be patterned, they are unable to take advantage of the simple processes and high temperatures that can be used with many organic materials. They also cannot be used for the single-step patterning of large areas, and they do not work well when applied to rough, uneven, or curved substrates. More recently, because of these and other limitations, a number of techniques and processes including unconventional lithography, non-impact printing (NIP), and traditional printing have been introduced for the fabrication of OTFT circuits and displays that aim specifically at reducing the fabrication cost.

In this study, fabrication processes were performed in device designs and experiments related to advanced organic material-TFTs, with an emphasis on now facing unconventional lithographic techniques. In particular, OTFTs were fabricated using microcontact printing, direct printing, and nanoimprint lithography at low process temperature. The OTFTs were used in the fabrication of a printed gate, source and drain electrodes, a coated poly-para-xylylene (Parylene) and polyvinylphenol (PVP) as the polymer gate dielectrics, and a solution-processed poly (3-hexylthiophene) (P3HT) and bis (triisopropyl-silylethynyl) pentacene (TIPS-pentacene) as the organic semiconductors on flexible, transparent plastic substrates. In addition to such more fabrication methods, conventional patterning processes-photolithography, screen printing, and roll printing-approaches have been developed.

The experiments and results were summarized fabrication OTFTs of study in (i) printed gate, source and drain electrodes of OTFTs were fabricated in the high resolution microcontact printing using poly (dimethylsiloxane) (PDMS) stamp and

self-assembled monolayers (SAMs) ink on poly(ethyleneterephthalate) (PEN) and PET plastic substrates, so that it was possible to fabricate a printed OTFT with channel lengths down to 1 μm , and reduce the fabrication process by 20 steps compared with photolithography, (ii) direct printing using patterned hard PDMS (h-PDMS) stamp, SAM solution, and low-viscosity conductive silver (Ag) ink, a printed OTFT with channel lengths of 5, 10, and 20 μm was fabricated on a 125 \times 125 mm substrate without pattern defects and the number of steps in the fabrication process was reduced by 30 steps compared with photolithography, and there were no need to carry out exposure, development, or removal processes, (iii) high-resolution and performance OTFTs with as small as 100 nm channel length was fabricated using ultra-violet nanoimprint lithography (UV-NIL) and thermal nanoimprint lithography onto Si/SiO₂ wafer substrate, (iv) OTFTs with channel lengths of 1, 5, and 10 μm were fabricated using photolithographic methods with lift-off or wet etching on 100 mm PEN plastic or liquid crystal display (LCD) glass substrate, (v) all printed OTFTs with channel length of as small as 14 μm were fabricated in the traditional technique based on screen printing from a fine mesh mask to a PEN, PET and PES substrates by squeezing using low-resistance Ag nanoparticle paste, (vi) to large-area patterning, with the device process in roll printing using plate engrave pattern mask, a printed OTFT with channel lengths of 50, 60, 70, and 80 μm fabricated, that have dimensions as 190 \times 395 mm.

Surface modification techniques were used to change the surface properties and enhance the performance. The electrical properties of the OTFTs were investigated using organic semiconductor fabricated by thermal evaporation and soluble process with the four kinds of dielectric surface treatments; as normal wet-cleaning, O₂ plasma treatment, hexamethyldisilazane ((CH₃)₃ SiOSi(CH₃)₃) (HMDS), SAMs, and octadecyltrichlorosilane (C₁₈H₃₇SiC₁₃) (OTS) treatment.

Since the fabrication of the printed OTFTs were carried out at near room temperature, it was possible to minimize dimensional distortion and to provide better alignment in the patterning process, thus preventing performance degradation. Also, during the device fabrication, there was no substrate shrinkage, bending, or pattern deformation.

As a result of evaluating the electrical characteristics of OTFTs fabricated by several patterning techniques, depending on the choice of fabrication methods, following parameters were obtained: the OTFTs have field-effect mobilities between 0.05 and 0.25 (± 0.03) cm²/Vs, an I_{on}/I_{off} ratio between 10² and 10⁵, I_{off} current below about 10⁻¹⁰ A, and a subthreshold slope between 1.26 and 12 V/decade.

This proposed unconventional lithographic technologies of using patterned electrodes and soluble organic semiconductors, combined with large-area stamping and printing techniques is believed to have the potential reduction of manufacturing costs by eliminating the need for photolithography.