Principal Researcher	Atsushi Iwata	**Number of Researchers**	6
Research Institution • Department • Title	Professor, Graduate School of Advanced Sciences of Matter, Hiroshima University	**Location of Institution**	Higashi-Hiroshima

Title of Project	3-dimensional integrated architecture with wireless chip-communication for high-recognition processing system
Abstract of Research Project	This is a research plan of circuit and system part in 21st century COE program "Tera bit information nano electronics". Although research and development in 3-dimensional integration technology has so far been done, several problems, such as chip penetration metal wiring, highly precise chip mount, heat radiation, low yield and so on, have not been solved. In order to solve these problems, the 3-dimensional integrated architecture with broadband wireless chip-communication is proposed. Flexible reconfiguration of 3-dimensional connection is enabled and the feature realizes the highly adaptive vision system and advanced brain functions based on information processing principle of the living body. 1. Wireless 3-dimensional integrated Chip Communication (1) Local connection: Many spiral antennas realize wireless communication between two chips placed in face-to-face. (2) Global connection: Integrated dipole antennas on silicon chips realize global connection beyond neighboring chips. The above connections realize Tera bit scale communication (3Gb/s x 300 channels) 2. High recognition processing system utilizing broadband wireless chip communication
References	1. H. Ando, T. Morie, M. Miyake, M. Nagata and A. Iwata, Image Segmentation/Extraction Using Nonlinear Cellular Networks and their VLSI Implementation Using Pulse-Modulation Techniques, IEICE Trans. Fundamentals, Vol. E85-A, No. 2, pp. 381-388, (2002). 2. S. Kinoshita, T. Morie, M. Nagata and A. Iwata, A PWM Analog Memory Programming Circuit for Floating-Gate MOSFETs with 75us Programming Time and 11b Updating Resolution, IEEE J. Solid-State Circuits, Vol. 36, No. 8, pp. 1286-1290, August, (2001).
Term of Project	Fiscal years 2003-2007 . (5years)

Budget Allocation (in thousand of yen)	FY2003	FY2004	FY2005	FY2006	FY2007	TOTAL
	18,700	16,700	17,500	16,600	16,600	86,100

Homepage Address	http://www.dsl.hiroshima-u.ac.jp/